IN THE CLAIMS:

Claims 9, 13-15, 18, and 19 have been amended herein. All of the pending claims 1 through 20 are presented below. This listing of claims will replace all prior versions and listings in the application. Please enter these claims as amended.

1. (Original) A method for electrically coupling a first side of a semiconductor substrate to a second side of said semiconductor substrate, comprising:

forming a hole having an inner surface from a first side of a semiconductor substrate to a second side of said semiconductor substrate; and

plating said inner surface of said semiconductor substrate to form a plated conductive element by forcing a plating solution from said first side of said semiconductor substrate to said second side of said semiconductor substrate through said hole.

2. (Original) The method of claim 1, wherein forming said hole comprises at least one of ablating, mechanically drilling and chemically etching a portion of said semiconductor substrate from said first side to said second side.

3. (Original) The method of claim 1, further comprising loading said semiconductor substrate into a plating fixture, said semiconductor substrate and said plating fixture cooperatively directing flow of a plating material through said hole of said semiconductor substrate.

4. (Original) The method of claim 1, wherein said plating comprises electroplating said inner surface of said semiconductor substrate defined by said hole.

5. (Original) The method of claim 1, wherein said plating process comprises electroless plating said inner surface of said semiconductor substrate defined by said hole.

6. (Original) The method of claim 1, further comprising forming a conductive cap on at least one end of said plated conductive element.

7. (Original) The method of claim 1, further comprising etching one of said first and second sides of said substrate to expose at least one end portion of said plated conductive element.

8. (Original) The method of claim 7, further comprising forming a conductive cap over said at least one end portion of said plated conductive element.

9. (Currently Amended) The method of claim 1, wherein said hole is between approximately ~~between~~ 50 microns and 700 microns in diameter.

10. (Original) A method of making a contactor card comprising:

forming a hole completely through a semiconductor substrate from a first side to a second side of said semiconductor substrate with an inner surface formed thereby; and

forcing a plating solution through said hole from a first plating bath to a second plating bath to deposit conductive material on said inner surface to form a first plated conductive element extending from said first side to said second side.

11. (Original) The method of claim 10, further comprising pulsing an electrical potential through said plating solution to induce deposit said conductive material on said inner surface.

12. (Original) The method of claim 10, further comprising forming a conductive cap on at least one end of said first plated conductive element.

13. (Currently Amended) The method of claim 10, further comprising coupling said semiconductor substrate into a plating fixture to provide a barrier around said semiconductor ~~wafer~~ substrate between said first bath and second bath.

14. (Currently Amended) The method of claim 10, further comprising etching at least one of said first and second sides of said substrate to expose at least one end portion of said first plated conductive element.

15. (Currently Amended) The method of claim 14, further comprising forming a conductive cap on said at least ~~a~~ one end portion of said first plated conductive element.

16. (Original) The method of claim 10, further comprising electrically coupling said first plated conductive element to a second plated conductive element over said semiconductor substrate.

17. (Original) A semiconductor substrate plating system, comprising:

a first plating fixture configured to receive a first semiconductor substrate including first and second sides and having at least one hole having an inner surface from said first side of said first semiconductor substrate to said second side of said first semiconductor substrate; and

a plating tank configured to receive said first plating fixture with said first semiconductor substrate therein, said first plating fixture and said first semiconductor substrate forming a partition within said plating tank of a higher pressure side with a higher pressure bath and a lower pressure side with a lower pressure bath with plating solution passing through said at least one hole from said higher pressure bath to said lower pressure bath and plating said inner surface of said at least one hole.

18. (Currently Amended) The semiconductor substrate plating system of claim 17, further comprising:

a second plating fixture configured to receive a second semiconductor substrate including first and second sides and having at least one hole having an inner surface from ~~a~~ said first side of said second semiconductor substrate to ~~a~~ said second side of said second semiconductor substrate; and

said plating tank further configured to receive said second plating fixture with said second semiconductor substrate therein, said second plating fixture and said second semiconductor substrate forming a partition within said plating tank of said lower pressure side with said lower pressure bath and a yet lower pressure side with a yet lower pressure bath with plating solution passing through said at least one hole from said lower pressure bath to said yet lower pressure bath and plating said inner surface of said at least one hole.

19. (Currently Amended) The semiconductor substrate plating system of claim 17, further comprising an electroplating arrangement configured within said plating tank and further configured to induce an electric field between said inner surface of said at least one hole of said first semiconductor substrate and said plating solution within said plating tank.

20. (Original) The semiconductor substrate plating system of claim 17, wherein said first plating fixture further has formed therein a bypass mechanism for passing said plating solution from said higher pressure bath to said lower pressure bath.

IN THE DRAWINGS:

The attached sheet of drawings includes a change to FIG. 7. This sheet, which includes FIG. 7, replaces the original sheet including FIGS. 7 and 8.